

In the claims:

Please amend the claims as follows:

Claims 1 to 17 have been withdrawn from consideration. Please cancel claims 1 to 17 without prejudice.

19. (Currently Amended) A semiconductor device comprising:

an upper layer wiring;

a pad portion disposed above the upper layer wiring;

an interlayer insulating film disposed below the upper layer wiring;

a lower layer wiring disposed below the interlayer insulating film; and

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a via-hole in the interlayer insulating film, connecting the upper layer wiring and the lower layer wiring; and a bump electrode provided at a pad portion covering lower layer wiring, wherein the via said hole is being formed not under but laterally spaced away from the pad portion,

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed under the pad portion formed at a region except under the bump electrode.

20. (Currently Amended) The semiconductor device according to claim 18 ~~19~~, wherein further comprising a lower layer wiring arranged ~~under~~ below the bump electrode.

21. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on a ~~semiconductor substrate through the~~ gate oxide film;

a source/drain region formed ~~so as to be in the semiconductor substrate and disposed~~ adjacent to the gate electrode;

~~a semiconductor region formed under the gate electrode and constituting a channel;~~

a lower layer wiring connected to the source/drain region with contact;

an interlayer insulating film covering the lower layer wiring;

a via-hole formed in an interlayer insulating film ~~covering the lower layer wiring and~~  
~~formed at a region except a bump electrode provided at a pad portion;~~ and

an upper layer wiring having a pad portion, disposed over the interlayer insulating film  
and connected to the lower layer wiring with contact through the via-hole,

wherein no hole connecting the upper layer wiring and the lower layer wiring is formed  
under the pad portion.

22. (Currently Amended) ~~The semiconductor device according to claim 21, further~~  
~~comprising~~ A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film provided over the semiconductor substrate;

a gate electrode formed on gate oxide film;

a source/drain region formed in the semiconductor substrate and disposed adjacent to the  
gate electrode;

a semiconductor region formed under the gate electrode comprising a channel;

a low concentration region of the same conductivity type as the source/drain region  
formed under the gate electrode so as to connect to the source/drain region and to contact the  
semiconductor region;

interlayer insulating film disposed over the gate electrode and the gate oxide film;

a lower layer wiring disposed in the interlayer insulating film and coupled to the  
source/drain region; and

an upper layer wiring disposed over the interlayer insulating film and coupled to the  
lower layer wiring through a hole in the interlayer insulating film.

23. (Currently Amended) A semiconductor device according to claim 21, ~~further~~  
~~comprising~~ wherein the low concentration region of the same conductivity type as the  
source/drain region formed extending extends shallowly to a surface layer of the semiconductor  
under the gate electrode so as to connect to the source/drain region and to contact the  
semiconductor region.

Claims 24 to 27 have been withdrawn from consideration. Please cancel ~~claims~~ 24 to 27 without prejudice.

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28. (New) The semiconductor device according to claim 21, wherein the interlayer insulating layer is provided with additional holes to couple the upper wiring to the lower layer wiring.

29. (New) The semiconductor device according to claim 19, wherein the interlayer insulating layer is provided with additional holes to couple the upper layer wiring to the lower layer wiring.

30. (New) The semiconductor device according to claim 19, further comprising a bump electrode provided at the pad portion.

31. (New) The semiconductor device according to claim 21, further comprising a semiconductor region formed under the gate electrode and constituting a channel.

32. (New) The semiconductor device according to claim 31, further comprising a bump electrode provided at the pad portion.

33. (New) The semiconductor device according to claim 21, further comprising a bump electrode provided at the pad portion.

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